Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-64. (Cancelled)

65. (currently amended):

A processor comprising: ~~The processor of claim 63 wherein:~~

an instruction delivery engine to store and fetch instructions to be executed by the processor from a plurality of threads based upon a current processing mode; and

an allocator to receive instructions from the instruction delivery engine and to perform allocation in a processor resource required for the execution of the instructions based upon the current processing mode, wherein the allocator,

if the current processing mode is single threading,

assigns all of the processor resource to one of the plurality of threads that is active,

~~the allocator~~ allocates an amount of entries for the instructions from the one of the plurality of threads in the processor resource if the processor resource has sufficient available entries, and ~~entries and wherein the allocator~~

activates at least one stall signal if the processor resource does not have sufficient available entries; and,

if the current processing mode is multithreading,

assigns a portion of the processor resource to each of the plurality of threads running concurrently,

~~the allocator~~ allocates an amount of entries for the instructions from each respective thread in a respective portion of the processor resource if the respective portion has sufficient available entries, and ~~entries and wherein the allocator~~

activates at least one stall signal if the respective portion does not have sufficient available entries.

66. (cancelled)

67. (previously presented):

The processor of claim 65 wherein the instruction delivery engine uses the at least one stall signal to perform its corresponding function.

68. (currently amended):

The processor of claim 67 wherein the instruction delivery engine re-fetches stalled instructions in the respective thread to the allocator if the at least one stall signal is activated.

4 ~~69~~. (original):

The processor of claim ~~67~~ 2 wherein the instruction delivery engine fetches a subsequent instruction from another thread to the allocator if the at least one stall signal for the respective thread is activated and said another thread is not stalled.

5 ~~70~~. (original):

The processor of claim ~~67~~ 2 wherein the instruction delivery engine fetches an invalid instruction to the allocator if the stall signal for the respective thread is activated.

71-85. (Cancelled)

6 ~~86~~. (currently amended):

A method for allocating processor resources by a processor, the method comprising: ~~The method of claim 85 wherein:~~

fetching instructions to be executed by the processor from one or more threads based upon a current processing mode; and,

performing allocation in a processor resource required for the execution of the instructions based upon the current processing mode, wherein performing allocation includes,

if the current processing mode is single threading,

assigning all of the processor resource to one of the plurality of threads that is active,

allocating an amount of entries for the instructions from the one of the plurality of threads in the processor resource if the processor resource has sufficient available entries, and

activating at least one stall signal if the processor resource does not have sufficient available entries; and,

if the current processing mode is multithreading,

assigning a portion of the processor resource to each of the plurality of threads running concurrently,

allocating an amount of entries for the instructions from each respective thread in a respective portion of the processor resource if the respective portion has sufficient available entries, and

activating at least one stall signal if the respective portion does not have sufficient available entries.

7 ~~87~~. (previously presented): 6

The method of claim ~~86~~ further comprising using the at least one stall signal to perform corresponding functions by the instruction delivery engine.

88. (currently amended):

The method of claim 87 further comprising re-fetching stalled instructions in the respective thread to the allocator if the at least one stall signal is activated.

89. (previously presented):

The method of claim 87 further comprising fetching a subsequent instruction from another thread to the allocator if the at least one stall signal for the respective thread is activated and said another thread is not stalled.

90. (previously presented):

The method of claim 87 further comprising fetching an invalid instruction to the allocator if the stall signal for the respective thread is activated.

91.-92. (cancelled):

93. (currently amended):

A processor comprising: ~~The processor of claim 92 wherein:~~

means for fetching instructions to be executed by the processor from one or more threads based upon a current processing mode;

means for performing allocation in a processor resource required for the execution of the instructions based upon the current processing mode;

means that are operative if the current processing mode is single threading for

assigning all of the processor resource to one of the plurality of threads that is active,

allocating an amount of entries for the instructions from the one of the plurality of threads in the processor resource if the processor resource has sufficient available entries, and

activating at least one stall signal if the processor resource does not have sufficient available entries; and,

means that are operative if the current processing mode is multithreading for

assigning a portion of the processor resource to each of the plurality of threads running concurrently,

allocating an amount of entries for the instructions from each respective thread in a respective portion of the processor resource if the respective portion has sufficient available entries, and

activating at least one stall signal if the respective portion does not have sufficient available entries.

94. (previously presented):

The processor of claim 93 further comprising means for using the at least one stall signal to perform corresponding functions by the instruction delivery engine.

13 ~~95.~~ (currently amended):

The processor of claim ~~94~~ 12 further comprising means for re-fetching stalled instructions in the respective thread to the allocator if the at least one stall signal is activated.

14 ~~96.~~ (previously presented):

The processor of claim ~~94~~ 12 further comprising means for fetching a subsequent instruction from another thread to the allocator if the at least one stall signal for the respective thread is activated and said another thread is not stalled.

15 ~~97.~~ (previously presented):

The processor of claim ~~94~~ 12 further comprising means for fetching an invalid instruction to the allocator if the stall signal for the respective thread is activated.

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